WE CLAIM:

1. A field effect device having a gate dielectric, wherein the gate dielectric comprises a germanate material.

2. The field effect device of claim 1, wherein the germanate material constitutes a layer.

3. The field effect device of claim 2, wherein the germanate material layer has a dielectric constant over 4.

4. The field effect device of claim 3, wherein the germanate material layer has a dielectric constant approximately between 8 and 40.

5. The field effect device of claim 2, wherein the germanate material layer has a thickness of approximately between 1.5nm and 50nm.

6. The field effect device of claim 1, further comprising a channel region, wherein the gate dielectric further comprises an interlayer disposed between the channel region and the germanate material layer.

7. The field effect device of claim 6, wherein the interlayer is less than approximately 1nm thick.

8. The field effect device of claim 1, wherein the gate dielectric consists essentially of the germanate material.

9. The field effect device of claim 1, wherein the gate dielectric comprising the germanate material possesses greater resistance against charge tunneling than a SiO_2 gate dielectric, and a capacitance per unit area of the gate dielectric comprising the germanate material is at least as large as the capacitance per unit area of the SiO_2 gate dielectric.

10. The field effect device of claim 1, wherein the germanate material is hafnium germanium oxide.

11. The field effect device of claim 1, wherein the field effect device is a Si MOS transistor.

12. The field effect device of claim 1, wherein the field effect device is a SiGe-based MOS transistor.

13. The field effect device of claim 1, wherein the field effect device is a Ge MOS transistor.

14. The field effect device of claim 1, wherein the field effect device is a III-V material based MOS transistor.

15. A method for fabricating a semiconductor field effect device comprising the step of:

forming a gate dielectric which comprises a germanate material having a chemical composition of $Me_zGe_xO_y$, where Me is a metal, and x, y, and z are non-zero integers.

16. The method of claim 15, further comprising the step of selecting the germanate material to withstand a temperature of at least 800°C.

17. The method of claim 15, further comprising the step of selecting the germanate material in a manner that the gate dielectric has greater resistance against charge tunneling than a SiO_2 gate dielectric, and a capacitance per unit area at least as large as the capacitance per unit area of the SiO_2 gate dielectric.

18. The method of claim 15, further comprising the step of providing a channel region to interface with the germanate material, and selecting the germanate material to provide interface stability with the channel region.

19. The method of claim 15, further comprising the step of providing a channel region to interface with the germanate material, and selecting the germanate material to maximize carrier mobility in the channel region.

20. The method of claim 15, further comprising the step of providing a source and a drain, wherein the step forming the gate dielectric is carried out before the step of providing the source and the drain.

21. The method of claim 15, further comprising the step of providing a source and a drain, wherein the step forming the gate dielectric is carried out after the step of providing the source and the drain.

22. The method of claim 15, wherein the germanate material is formed by a chemical vapor deposition technique.

23. The method of claim 22, wherein the chemical vapor deposition is performed in a temperature range of between about 300°C and 700°C.

24. The method of claim 15, wherein the germanate material is formed by atomic layer deposition.

25. The method of claim 24, wherein the atomic layer deposition comprises between about 10 and 500 cycles of layer deposition.

26. A processor, comprising:

at least one chip, wherein the chip comprises at least one semiconductor field effect device having a gate dielectric, wherein the gate dielectric comprises a germanate material.

27. The processor of claim 26, wherein the processor is a digital processor.

28. The processor of claim 26, wherein the processor comprises at least one analog circuit.